REMARKS

Filing of RCE

Applicants have filed a Request for Continued Examination (RCE) before payment of the issue fee in accordance with 37 C.F.R. 1.114(a)(1) in order to reopen prosecution of the application. New claims 170-175 have been added by the present amendment as the submission required to be filed with the RCE under 37 C.F.R. 1.114(c).

Pending Claims

Claims 164-175 are pending. Claims 164-169 were allowed in the Notice of Allowance mailed March 16, 2005. New claims 170-175 are respectfully asserted to be allowable over the art of record for the following reasons.

Claims 170-175 are substantially similar to claims 164-169, with the following exception. Claims 164, 168 and 169 set forth that the predetermined unit time, which is common to all of the plurality of the processing apparatuses and the inter-apparatus transporter, is (1) longer than the shortest required time for either processing in each of the processing apparatuses or for transporting by the inter-apparatus

transporter, but is (2) shorter than the longest required time for either processing in each of the processing apparatuses or for transporting by the inter-apparatus transporter. In claims 170, 174 and 175, the first of these two limitations, i.e. that the predetermined unit time is longer than the shortest required time for either processing in each of the processing apparatuses or for transporting by the inter-apparatus transporter, has been deleted. Accordingly, claims 170, 174 and 175 set forth the second limitation in common with claims 164, 168 and 169, i.e. that the predetermined unit time is shorter than the longest required time for either processing in each of the processing apparatuses or for transporting by the inter-apparatus transporter, however not the first limitation.

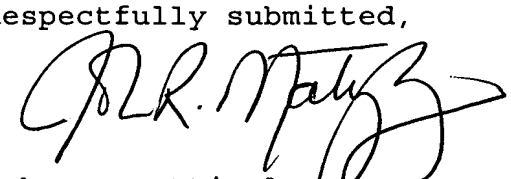
Applicants respectfully assert that claims 170-175 are patentable over the art of record and, in particular, over Nishida et al (Nishida), U.S. Patent No. 5,436,848. Nishida discloses driving a robot 5, which transports semiconductor wafers, according to a single constant cycle time. The cycle time that is chosen is that of the longest process. Accordingly, the reference does not disclose the claimed time

interval(s) in relation to a predetermined unit time that is shorter than the longest required time for either processing in each of the processing apparatuses or for transporting with the inter-apparatus transporter. In Nishida, wafers are transported between processes in a predetermined amount of time, then a waiting time is provided so that transporting of the wafers between processes is conducted within the cycle time. Accordingly, Nishida does not disclose or suggest the invention of claims 170-175. Further, these claims are patentable over the remainder of the art of record at least for the same reasons that claims 164-169 were found to be allowable as indicated in the Notice of Allowance.

Conclusion

Applicants request examination of the pending claims in view of the foregoing remarks.

Respectfully submitted,



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